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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/699,077	10/27/2000	Masahiro Ishida	KPO089	9031

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EXAMINER	
SHARON, AYAL I	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/699,077	ISHIDA ET AL.
	Examiner	Art Unit
	Ayal I Sharon	2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,6 and 8-12* is/are rejected.

7)☒ Claim(s) *3,5 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/19/2004*.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Introduction

1. Claims 1-12 of U.S. Application 09/699,077, originally filed on 10/27/2000, are presented for examination. The application has a foreign priority date of 01/24/2000. In the most recent response from the Applicants, filed on 8/3/2004, Applicants have amended p.10 of the specification to correct a misspelled word ("ration" is changed to "ratio"), but have not amended, added, or cancelled any claims. In response to Applicants' arguments,

Allowable Subject Matter

2. Claims 3, 5, and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and all intervening claims.

3. In regards to Claim 3,

> 3. The method of claim 2, wherein said fault list generating step is a step of checking, for said each logic gate, whether a logic signal value sequence in an output signal line of said each logic gate has been changed, and if so, generating said fault list in which an identifier of a test pattern sequence having changed said logic signal value sequence and said logic gate are registered in correspondence with each other.

neither Cole, Acuna, or Carmeichel, either individually nor in combination, teach the combination of limitations in this claim.

4. In regards to Claim 5,

> 5. The method of claim 4, wherein said fault list generating step comprising the steps of:

checking, for said each signal line, whether said logic signal value sequence in said each signal line has been changed;

if so, checking whether a logic signal value sequence in an output signal line of a logic gate having its input connected to said signal line, in which said logic signal value sequence has been changed, is changed by a test pattern sequence having changed said logic signal value sequence in said signal line, and if so, generating said fault list in which said signal line and an identifier of said test pattern sequence having changed said logic signal value sequence in said signal line are registered in correspondence with each other.

neither Cole, Acuna, or Carmeichel, either individually nor in combination, teach the combination of limitations in this claim.

5. In regards to Claim 7,

7. The method of claim 6, wherein said fault list generating step is a step of checking, for said each signal propagation path, whether logic signal value sequences at respective points in said each signal propagation path have all been changed, and if so, generating said fault list in which an identifier of a test pattern sequence having changed said logic signal value sequences and said each signal propagation path are registered in correspondence with each other.

neither Cole, Acuna, or Carmeichel, either individually nor in combination, teach the combination of limitations in this claim.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The prior art used for these rejections is as follows:

8. Cole, Jr. et al. U.S. Patent 6,031,386. (Henceforth referred to as "**Cole**").

9. Acuna, E.L. et al. "Simulation Techniques for Mixed Analog / Digital Circuits." IEEE Journal of Solid-State Circuits. Vol.25, Issue 2. pp.353-363. (Henceforth referred to as "**Acuna**").

10. Carmichael, N. et al. "Simulation as an Aid to Power Supply Diagnostics". AUTOTESTCON '95. Aug. 8-10, 1995. pp.556-560. (Henceforth referred to as "**Carmichael**").

11. **Claims 1-2, 4, 6, and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cole in view of Acuna.**

12. In regards to Claim 1, Cole teaches the following limitations of Claim 1:

1. A fault simulation method for a semiconductor IC, said method comprising the steps of:

generating a test pattern sequence composed of two or more test patterns for input to said semiconductor IC;

(Cole, especially: col.2, line 65 to col.3, line 5. Cole teaches "[a] means connected to a plurality of input pins or terminals of the IC for providing a vector set of voltage inputs to the IC for toggling the IC between logic states thereof."

Also, Cole, col.3, lines 17-20. Cole teaches that "The means for providing the vector set of voltage inputs to the IC can comprise a switch matrix, or preferably an integrated circuit tester."

Examiner interprets Applicants' "test pattern sequence" as being a duplication of Cole's "vector set of voltages".)

performing a logic simulation of the operation of said semiconductor IC in the case of applying thereto each of said two or more test patterns of said test pattern sequence, and calculating a logic signal value sequence in each signal line in said semiconductor IC; and

(Cole, especially: col.3, lines 40-46. Cole teaches "... and identifying ICs having defects or failure mechanisms therein by determining whether the transient voltage component V_{DDT} exceeds a known value. The known value can be derived from measurements of one or more defect-free ICs using the present invention, or derived from numerical modeling of electrical characteristics of the IC (i.e. from modeling of a design for the IC).")

generating a list of faults, which are detectable by a transient power supply current testing using said test pattern sequence, through the use of said logic signal value sequence in said each signal line calculated by said logic simulation.

(Cole, especially: col.3, lines 35-46. Cole teaches "toggling the IC between logic states by providing a vector set of voltage inputs to input pins of the IC ...

and identifying ICs having defects or failure mechanisms therein by determining whether the transient voltage component, V_{DDT} exceeds a known value.)

Examiner notes that Cole teaches two embodiments of his invention: 1) measuring a transient voltage component V_{DDT} (col.3, lines 32-46) and 2) measuring a time delay in a transient voltage component V_{DDT} (col.3, lines 48-62). In both embodiments, the measured values are compared to "known values" derived from numerical modeling of the IC.

However, Cole does not expressly teach that the numerical modeling that is performed is a "logic simulation" as opposed to a "transition simulation", as defined by Applicants in paper #4, p.7. (Applicants defined the difference between the two types of simulation as follows: "A transition simulation must account for the timing of signal transitions …", while "A logic simulation does not need to account for the timing of signal transitions. It considers state logic levels.")

Acuna, on the other hand, teaches a simulator which performs four types of circuit simulation (see Acuna, Section II, pp.354-355): 1) Electrical Analysis, 2) Logic Analysis, 3) Electrical-Logical (ELOGIC) Analysis, and 4) Time Step Synchronization.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Cole with those of Acuna, because Acuna teaches the use of both analog and digital simulation of mixed analog/digital MOS circuits (see Acuna, Abstract), which is what is needed to

simulate the MOS circuits in Cole's "numerical modeling" step (see Cole, col.3, lines 42-46).

13. In regards to Claim 2,

2. The method of claim 1, wherein said fault list generating step is a step of generating said fault list for each logic-gate in said semiconductor IC.

Cole teaches that measured values are compared to "known values" derived from numerical modeling of the IC. Cole also teaches (see col.3, lines 35-46) "... toggling the IC between logic states by providing a vector set of voltage inputs to input pins of the IC ... and identifying ICs having defects or failure mechanisms therein by determining whether the transient voltage component, V_{DDT} exceeds a known value."

Examiner interprets that the list of "defects or failed mechanism" constitutes a "fault list".

However, Cole does not expressly teach that this list is created "for each logic gate in said semiconductor IC."

Acuna, on the other hand, teaches (see Section "II.B Logic Analysis") that "Inertial delay models are used <u>for all gates</u> except for the pass transistor. The delay can be specified as <u>fixed values or fan-out-dependent values</u> which depend on the output capacitive loading."

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Cole with those of Acuna, because Acuna teaches the use of both analog and digital simulation of mixed analog/digital MOS circuits (see Acuna, Abstract), which is above and beyond

what is needed to simulate the MOS circuits in Cole's "numerical modeling" step (see Cole, col.3, lines 42-46).

14. In regards to Claim 4,

4. The method of claim 1, wherein said fault list generating step is a step of generating said fault list for said each signal line.

Cole teaches that measured values are compared to "known values" derived from numerical modeling of the IC. Cole also teaches (see col.3, lines 35-46) "... toggling the IC between logic states by providing a vector set of voltage inputs to input pins of the IC ... and identifying ICs having defects or failure mechanisms therein by determining whether the transient voltage component, V_{DDT} exceeds a known value."

Examiner interprets that the list of "defects or failed mechanism" constitutes a "fault list".

However, Cole does not expressly teach that this list is created "for each signal line."

Acuna, on the other hand, teaches (see Section "II.B Logic Analysis") that "Inertial delay models are used <u>for all gates</u> except for the pass transistor. The delay can be specified as <u>fixed values or fan-out-dependent values</u> which depend on the output capacitive loading."

Examiner interprets that the <u>gate information</u> applies to the corresponding <u>signal lines</u> attached to the gates.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Cole with those of Acuna,

because Acuna teaches the use of both analog and digital simulation of mixed analog/digital MOS circuits (see Acuna, Abstract), which is above and beyond what is needed to simulate the MOS circuits in Cole's "numerical modeling" step (see Cole, col.3, lines 42-46).

15. In regards to Claim 6,

> 6. The method of claim 1, wherein said fault list generating step is a step of generating said fault list for each signal propagation path in said semiconductor IC.

Cole teaches that measured values are compared to "known values" derived from numerical modeling of the IC. Cole also teaches (see col.3, lines 35-46) "... toggling the IC between logic states by providing a vector set of voltage inputs to input pins of the IC ... and identifying ICs having defects or failure mechanisms therein by determining whether the transient voltage component, V_{DDT} exceeds a known value."

Examiner interprets that the list of "defects or failed mechanism" constitutes a "fault list".

However, Cole does not expressly teach that this list is created "for each signal propagation path in said semiconductor IC."

Acuna, on the other hand, teaches (see Section "II.B Logic Analysis") that "Inertial delay models are used <u>for all gates</u> except for the pass transistor. The delay can be specified as <u>fixed values or fan-out-dependent values</u> which depend on the output capacitive loading."

Examiner interprets that the <u>gate information</u> applies to the corresponding <u>signal lines</u> ("<u>signal propagation paths</u>") attached to the gates.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Cole with those of Acuna, because Acuna teaches the use of both analog and digital simulation of mixed analog/digital MOS circuits (see Acuna, Abstract), which is above and beyond what is needed to simulate the MOS circuits in Cole's "numerical modeling" step (see Cole, col.3, lines 42-46).

16. In regards to Claim 8,

8. The method of claim 1, further comprising the step of calculating said logic signal value sequence for every test pattern sequence prior to said fault list generating step.
(Examiner finds this to be inherent. There is a fault if the logic signal value is incorrect. Therefore, the expected logic signals must be calculated first, before testing for faults, or listing the located faults.)

17. In regards to Claim 9,

9. The method of claim 1, further comprising the step of calculating said logic signal value sequence and generating said fault list upon generation of each test pattern sequence.
(Examiner finds this to be inherent. Just as the expected logic signals must be calculated first, before testing for faults, it is also true that the logic signal value can only be calculated after the test pattern has been inputted.)

18. In regards to Claim 10, Cole teaches the following limitations of Claim 10:

10. A fault simulator for a semiconductor IC, comprising:
test pattern generating means for generating a test pattern sequence composed of two or more test patterns for input to said semiconductor IC;
(Cole, especially: col.2, line 65 to col.3, line 5. Cole teaches "[a] means connected to a plurality of input pins or terminals of the IC for providing a vector set of voltage inputs to the IC for toggling the IC between logic states thereof."
Also, Cole, col.3, lines 17-20. Cole teaches that "The means for providing the vector set of voltage inputs to the IC can comprise a switch matrix, or preferably an integrated circuit tester."
Examiner interprets Applicants' "test pattern sequence" as being a mere duplication of Cole's "vector set of voltages".)

a logic simulator supplied with said test pattern sequence, for performing a logic simulation of the operation of said semiconductor IC in the case of applying thereto each of said two or more test patterns, and for calculating and outputting a logic signal value sequence in each signal line in said semiconductor IC;

(Cole, especially: col.3, lines 40-46. Cole teaches "... and identifying ICs having defects or failure mechanisms therein by determining whether the transient voltage component V_{DDT} exceeds a known value. The known value can be derived from measurements of one or more defect-free ICs using the present invention, or derived from numerical modeling of electrical characteristics of the IC (i.e. from modeling of a design for the IC).")

a memory for storing said calculated logic signal value sequence generated in said each signal line for each test pattern sequence; and

(Examiner finds it is inherent that Cole has a memory for storing the "vector set of voltages", in order to keep track of what is being input for the test. Otherwise it would be impossible to keep track of which inputs generated faults.

Since Examiner interprets Applicants' "test pattern sequence" as being a mere duplication of Cole's "vector set of voltages", and that Cole has a memory for storing the "vector set of voltages", in order to keep track of what is being input for the test, it is inherent that Cole would have a memory for the "test pattern sequence". Otherwise it would be impossible to keep track of which inputs generated faults.)

fault list generating means supplied with said logic signal value sequence of said each signal line stored in said memory, for generating a list of faults detectable by a transient power supply current testing using said test pattern sequence.

(Cole, especially: col.3, lines 35-46. Cole teaches "toggling the IC between logic states by providing a vector set of voltage inputs to input pins of the IC ... and identifying ICs having defects or failure mechanisms therein by determining whether the transient voltage component, V_{DDT} exceeds a known value.)

Examiner notes that Cole teaches two embodiments of his invention: 1) measuring a transient voltage component V_{DDT} (col.3, lines 32-46) and 2) measuring a time delay in a transient voltage component V_{DDT} (col.3, lines 48-62). In both embodiments, the measured values are compared to "known values" derived from numerical modeling of the IC.

However, Cole does not expressly teach that the numerical modeling that is performed is a "logic simulation" as opposed to a "transition simulation", as defined by Applicants in paper #4, p.7. (Applicants defined the difference between the two types of simulation as follows: "A transition simulation must

account for the timing of signal transitions ...", while "A logic simulation does not need to account for the timing of signal transitions. It considers state logic levels.")

Acuna, on the other hand, teaches a simulator which performs four types of circuit simulation (see Acuna, Section II, pp.354-355): 1) Electrical Analysis, 2) Logic Analysis, 3) Electrical-Logical (ELOGIC) Analysis, and 4) Time Step Synchronization.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Cole with those of Acuna, because Acuna teaches the use of both analog and digital simulation of mixed analog/digital MOS circuits (see Acuna, Abstract), which is what is needed to simulate the MOS circuits in Cole's "numerical modeling" step (see Cole, col.3, lines 42-46).

19. **Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cole in view of Carmichael.**

20. In regards to Claim 11, Cole teaches the following limitations of Claim 11 (except for the limitations in bold italics):

11. A fault simulation method for a semiconductor IC, said method comprising the steps of:
inserting an assumed fault in said semiconductor IC;

generating a test pattern sequence composed of two or more test patterns for input to said semiconductor IC;

(Cole, especially: col.2, line 65 to col.3, line 5. Cole teaches "[a] means connected to a plurality of input pins or terminals of the IC for providing a vector set of voltage inputs to the IC for toggling the IC between logic states thereof."

Also, Cole, col.3, lines 17-20. Cole teaches that "The means for providing the vector set of voltage inputs to the IC can comprise a switch matrix, or preferably an integrated circuit tester."

Examiner interprets Applicants' "test pattern sequence" as being a duplication of Cole's "vector set of voltages".)

applying said test pattern to said semiconductor IC ***with said assumed fault inserted therein*** and performing a circuit simulation of the operation of said semiconductor IC to thereby calculate a transient power supply current of said semiconductor IC;

(Cole, especially: col.3, lines 40-46. Cole teaches "... and identifying ICs having defects or failure mechanisms therein by determining whether the transient voltage component V_{DDT} exceeds a known value. The known value can be derived from measurements of one or more defect-free ICs using the present invention, or derived from numerical modeling of electrical characteristics of the IC (i.e. from modeling of a design for the IC).")

comparing said calculated transient power supply current with the transient power supply current of a normal circuit and ***deciding whether said assumed fault is detectable*** by a transient power supply current testing using said test pattern sequence; and

(Cole, especially: col.3, lines 40-46. Cole teaches "... and identifying ICs having defects or failure mechanisms therein by determining whether the transient voltage component V_{DDT} exceeds a known value. The known value can be derived from measurements of one or more defect-free ICs using the present invention, or derived from numerical modeling of electrical characteristics of the IC (i.e. from modeling of a design for the IC).")

generating a fault list ***in which said detectable fault*** and an identifier of said test pattern sequence are registered.

(Cole, especially: col.3, lines 35-46. Cole teaches "toggling the IC between logic states by providing a vector set of voltage inputs to input pins of the IC ... and identifying ICs having defects or failure mechanisms therein by determining whether the transient voltage component, V_{DDT} exceeds a known value.)

However, Cole does not expressly teach that an assumed fault is inserted into the semiconductor IC, that the test pattern is applied to the semiconductor IC with the assumed fault inserted therein, deciding whether the assumed fault is detectable, or generating a fault list in which the detectable faults are registered.

Carmichael, on the other hand, does teach the insertion of assumed faults into the semiconductor IC (see Section II.A. "Simulation Process"), as well as applying the test pattern is applied to the semiconductor IC with the assumed fault inserted therein (see Section III.A. "Switching Regulator Example"), deciding

whether the assumed fault is detectable (see Section III.A. "Switching Regulator Example"), and generating a fault list in which the detectable faults are registered (see Section III.A. "Switching Regulator Example").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Cole with those of Carmichael, because "simulation allows a fault to be inserted without damaging the power supply under test. This benefit is particularly important because failures in power supplies often have an avalanche effect. One failure can propagate to damage several other components." (see Carmichael, "Abstract").

21. In regards to Claim 12, Cole teaches the following limitations of Claim 12 (except for the limitations in bold italics):

12. A fault simulator for a semiconductor IC comprising:

test pattern generating means for generating a test pattern sequence composed of two or more test patterns for input to said semiconductor IC;

(Cole, especially: col.2, line 65 to col.3, line 5. Cole teaches "[a] means connected to a plurality of input pins or terminals of the IC for providing a vector set of voltage inputs to the IC for toggling the IC between logic states thereof."

Also, Cole, col.3, lines 17-20. Cole teaches that "The means for providing the vector set of voltage inputs to the IC can comprise a switch matrix, or preferably an integrated circuit tester."

Examiner interprets Applicants' "test pattern sequence" as being a duplication of Cole's "vector set of voltages".)

fault inserting means for inserting an assumed fault into said semiconductor IC;

a circuit simulator for applying said test pattern to said semiconductor IC with said ***assumed fault inserted therein*** and performing a circuit simulation of the operation of said semiconductor IC to thereby calculate a transient power supply current of said semiconductor IC;

(Cole, especially: col.3, lines 40-46. Cole teaches "... and identifying ICs having defects or failure mechanisms therein by determining whether the transient voltage component V_{DDT} exceeds a known value. The known value can be derived from measurements of one or more defect-free ICs using the

present invention, or derived from numerical modeling of electrical characteristics of the IC (i.e. from modeling of a design for the IC).")

> and fault list generating means for comparing said calculated transient power supply current with the transient power supply current of a normal circuit, ***for deciding whether said assumed fault is detectable*** by a transient power supply current testing using said test pattern sequence, and for registering said detectable fault and an identifier of said test pattern sequence in a fault list.

(Cole, especially: col.3, lines 35-46. Cole teaches "toggling the IC between logic states by providing a vector set of voltage inputs to input pins of the IC … and identifying ICs having defects or failure mechanisms therein by determining whether the transient voltage component, V_{DDT} exceeds a known value.)

However, Cole does not expressly teach that an assumed fault is inserted into the semiconductor IC, that the test pattern is applied to the semiconductor IC with the assumed fault inserted therein, deciding whether the assumed fault is detectable, or generating a fault list in which the detectable faults are registered.

Carmichael, on the other hand, does teach the insertion of assumed faults into the semiconductor IC (see Section II.A. "Simulation Process"), as well as applying the test pattern is applied to the semiconductor IC with the assumed fault inserted therein (see Section III.A. "Switching Regulator Example"), deciding whether the assumed fault is detectable (see Section III.A. "Switching Regulator Example"), and generating a fault list in which the detectable faults are registered (see Section III.A. "Switching Regulator Example").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Cole with those of Carmichael, because "simulation allows a fault to be inserted without damaging the power supply under test. This benefit is particularly important because failures in power

supplies often have an avalanche effect. One failure can propagate to damage several other components." (see Carmichael, "Abstract").

Response to Arguments

Re: Amendment to the Specification

22. In the paper filed on 8/3/2004, the Applicants have made a minor amendment to p.10 of the specification which clarifies an error in the translation from the original Japanese text. Examiner finds that this do not constitute new matter, and has entered these amendments.

Re: IDS

23. Examiner thanks the Applicants for raising the issue of the unsigned IDS. A signed copy of the IDS form is attached to this Office Action. While the reference cited in that IDS has not been used as a grounds for rejection in this Office Action, the Examiner finds the art to be relevant and reserves the right to cite this reference in the future.

Re: Claim Rejections - 35 USC § 103

24. Applicants unpersuasively argue (paper filed 8/3/2004, p.4, para.1) that:

> "... the method of claim 1 is not directed toward testing semiconductor ICs *per se*. Claim 1 recites steps of a method for generating a list of faults in a semiconductor IC that are capable of being detected by transient power supply testing. The method of claim 1 does not actually test an IC but instead produces a list of faults that may be used to design a set of test patterns for more efficient testing."

Among the limitations of Claim 1 is the following limitation:

> "...performing a logic simulation of the operation of said semiconductor IC in the case of applying thereto each of said two or more test patterns of said test pattern sequence, and calculating a logic signal value sequence in each signal line in said semiconductor IC ..."

Examiner finds that "...performing a logic simulation of the operation of said semiconductor IC in the case of applying thereto each of said two or more test patterns ..." corresponds to a form of testing semiconductor ICs, due to the "applying" of "test patterns" to the circuit.

25. Applicants unpersuasively argue (paper filed 8/3/2004, p.4, para.2) that:

> "... Cole does not teach anything that allows a person of ordinary skill in the art to determine which faults are capable of being detected by its disclosed methods of testing or by any other methods of testing."

Examiner refers the Applicants to col.4, lines 59-64 of Cole, which teaches (emphasis added):

> "The transient voltage component V_{DDT} is used to provide an indication of any defects present within each IC 100 being tested by the apparatus 10, <u>and in particular defects that alter an electrical current to the IC 100.</u>"

26. Applicants unpersuasively argue (paper filed 8/3/2004, p.4, para.3) that:

> "Furthermore, neither Cole nor Acuna disclose or suggest the second step recited in claim 1 in which two or more test patterns are applied to calculate logic value sequences in each signal line of an IC."

Examiner refers the Applicants to col.5, lines 13-17, which teach:

> "In Fig.1, the IC tester 14 provides the test vector set to the IC 100 via a plurality of input lines 16 connected to the voltage input pins of the IC, and also preferably reads out the logic states of the IC 100 via a plurality of output lines 18 connected to the voltage output pins of the IC."

In addition, Examiner refers the Applicants to col.5, lines 24-34, which teach:

> "In using the present invention, it is generally not desirable to individually test every transistor gate in the IC 100 for defects or failure mechanisms. This is especially the case in a production environment where the goal is to qualify large numbers of ICs as being substantially free of defects or failure mechanisms, while minimizing the time required for testing. The set of test vectors can be determined from the design of a particular IC 100, and an exact set of test vectors can vary depending on whether the apparatus 10 is to be used for production testing, or for failure analysis."

Examiner finds that "signal line of an IC" corresponds to the "output lines" lines of an IC, and not to "transistor gates".

27. Applicants unpersuasively argue (paper filed 8/3/2004, p.4, para.3) that:

> "Carmichael discusses research in which engineers simulated operation of a power supply circuit with a numerical model and used this model as an aid to determine manually how several assumed faults affected circuit operation. There is no teaching or suggestion for any technique that determines whether a particular fault can be detected by transient power supply current testing. Indeed, this type of testing is not even mentioned."

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

28. Applicant's arguments filed 8/3/2004 have been fully considered but they are not persuasive.

29. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (571) 272-3714. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached at (571) 272-3716.

Any response to this office action should be faxed to (703) 872-9306 or mailed to:

Director of Patents and Trademarks
Washington, DC 20231

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center 2100 Receptionist, whose telephone number is (571) 272-2100.

Ayal I. Sharon

Art Unit 2123

October 27, 2004

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER